AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A digital microphone comprising:

a microphone housing having a sound inlet and comprising:

a transducer element comprising a displaceable diaphragm and adapted to generate a transducer signal representative of sound received through the sound inlet,

an analog-to-digital converter comprising a multi-level quantizer operatively coupled to the transducer element to convert the transducer signal into multi-bit samples representative of the transducer signal, the multi-level quantizer having at least three discrete quantization levels, each of the discrete quantization levels being represented by a set of corresponding symbols, each symbol comprises a number of one signs, the number of one signs being proportional with a magnitude of the transducer signal represented by the corresponding multi-bit sample,

a digital signal converter adapted to convert the multi-bit samples into an unformatted single-bit output signal, and

an externally accessible terminal adapted to provide the unformatted single-bit output signal.

2. (Previously Presented) A digital microphone according to claim 1, wherein the analog-to digital converter comprises an oversampled delta-sigma modulator.

3. (Previously Presented) A digital microphone according to claim 1, comprising an integral clock generator operatively coupled to the analog-to-digital converter and the digital signal converter.

4. (Previously Presented) A digital microphone according to claim 1, wherein the microphone housing comprises a second externally accessible terminal for receipt of an external clock signal.

5. (Previously Presented) A digital microphone according to claim 4, comprising a DC voltage generating means for deriving a DC voltage supply for operating at least the analog-to-digital converter, the DC voltage supply means being disposed within the microphone housing and operatively coupled to the external clock signal.

6. (Previously Presented) A digital microphone according to claim 1, wherein the multi-level quantizer of the analog-to-digital converter comprises between 3 and 64 discrete quantization levels.

7. (Previously Presented) A digital microphone according to claim 1, wherein the multi-bit samples provided by the analog-to-digital converter are represented in two's complement format.

8. (Canceled)

9. (Previously Presented) A digital microphone according to claim 1, wherein the multi-level quantizer comprises 3 or 5 discrete quantization levels.

10. (Previously Presented) A digital microphone according to claim 1, wherein the multi-level quantizer comprises N discrete quantization levels and each corresponding symbol comprises N-1 bits; N being an integer between 3 and 17.

11. (Previously Presented) A digital microphone according to claim 9, wherein the digital signal converter comprises a delay circuit in cascade with an integer ratio upsampler.

12. (Previously Presented) A digital microphone according to claim 1, comprising a preamplifier interposed between the transducer element and the analog-to-digital converter.

13. (Previously Presented) A digital microphone according to claim 1, comprising an interpolator operatively coupled between the multi-bit samples provided by the analog-to-digital converter and the digital signal converter.

14. (Previously Presented) A portable communication device comprising a digital microphone according to claim 1.

15. (Previously Presented) A monolithic integrated circuit for a miniature microphone, comprising:

a preamplifier adapted to provide an amplified transducer signal and comprising an input section couplable to a miniature electret or condenser transducer element,

an analog-to-digital converter comprising a multilevel-quantizer operatively coupled to the amplified transducer signal and adapted to convert the amplified transducer signal into multi-bit samples representative of the amplified transducer signal, the multi-level quantizer having at least three discrete quantization levels, each of the discrete quantization levels being represented by a set of corresponding symbols, each symbol comprises a number of one signs, the number of one signs being proportional with a magnitude of the transducer signal represented by the corresponding multi-bit sample,

a digital signal converter adapted to convert the multi-bit samples into an unformatted single-bit output signal, and

an integrated circuit pad adapted to provide the single-bit output signal.

16. (Canceled)

17. (Previously Presented) A monolithic integrated circuit according to claim 15, wherein the analog-to-digital converter comprises an oversampled delta-sigma modulator.

18. (Previously Presented) A monolithic integrated circuit according to claim 15, wherein the multi-level quantizer of the analog-to-digital converter comprises 3 or 5 discrete quantization levels.

19. (Previously Presented) A digital microphone according to claim 1, wherein the digital signal converter is a sigma-delta signal converter.

20. (Previously Presented) A digital microphone according to claim 1, wherein:

the analog-to-digital converter is a tri-level sigma-delta modulator, the tri-level sigma-delta modulator outputs two bit samples in standard two's format, and

the digital signal converter comprises a first D-type Flip Flop, a second D-type Flip Flop, a third D-type Flip Flop, a fourth D-type Flip Flop, a dual-input multiplexer and an XOR gate, where:

the first D-type Flip Flop receives a clock frequency from a clock input and outputs a half frequency, the half frequency being half of the clock frequency,

the second D-type Flip Flop receives and operates on the half frequency, the second D-type Flip Flop further receives a first of the two bit samples from the analog-to-digital converter, the second D-type Flip Flop outputs from a non-inverted output a first signal,

the third D-type Flip Flop receives and operates on the half frequency, the third D-type Flip Flop further receives a second of the two bit samples from the analog-to-digital converter, the third D-type Flip Flop outputs a second signal from a non-inverted output and a third signal from an inverted output,

the XOR gate receives the first and second signals and outputs a fourth signal,

the multiplexer receives and operates on the half frequency, the multiplexer further receives the third and fourth signals, the multiplexer outputs a fifth signal,

the fourth D-type Flip Flop receives the clock frequency and the fifth signal signal, the fourth D-type Flip Flop outputs the unformatted single-bit output signal.

21. (Previously Presented) A monolithic integrated circuit according to claim 15, wherein:

the analog-to-digital converter is a tri-level sigma-delta modulator, the tri-level sigma-delta modulator outputs two bit samples in standard two's format, and

the digital signal converter comprises a first D-type Flip Flop, a second D-type Flip Flop, a third D-type Flip Flop, a fourth D-type Flip Flop, a dual-input multiplexer and an XOR gate, where:

the first D-type Flip Flop receives a clock frequency from a clock input and outputs a half frequency, the half frequency being half of the clock frequency,

the second D-type Flip Flop receives and operates on the half frequency, the second D-type Flip Flop further receives a first of the two bit samples from the analog-to-digital converter, the second D-type Flip Flop outputs from a non-inverted output a first signal,

the third D-type Flip Flop receives and operates on the half frequency, the third D-type Flip Flop further receives a second of the two bit samples from the analog-to-digital converter, the third D-type Flip Flop outputs a second signal from a non-inverted output and a third signal from an inverted output,

the XOR gate receives the first and second signals and outputs a fourth signal,

the multiplexer receives and operates on the half frequency, the multiplexer further receives the third and fourth signals, the multiplexer outputs a fifth signal,

the fourth D-type Flip Flop receives the clock frequency and the fifth signal signal, the fourth D-type Flip Flop outputs the unformatted single-bit output signal.